INDUSTRIAL MICRO SYSTEMS INC.

MODEL 370

32K STATIC RAM MEMORY BOARD

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The 370 RAM board is fully static and fully buffered and provides 32K bytes of memory organized into 8 contiguous blocks of 4K bytes each. The starting address of the 32K bytes may be located at any 4K boundry. Each 4K block may be individually turned "ON" or "OFF" to provide full mapping capabilities for use in systems utilizing Memory Management.

A "Phantom Line" option is provided for use in systems with ROM memories which utilize this feature. The user may also select the Processor Write (PWR) signal or the Memory Write (MWR) signal as the data strobe for storing data providing for full compatibility with front panels.

The 370 Static RAM board has been manufactured to Industrial standards which include rigorous inspections and testing including dynamic "burn-in" testing at 70 degrees C. All components have been carefully selected to provide long, trouble free service.

CONFIGURING THE 370 BOARD

STARTING ADDRESS

The starting address of the memory board is determined by the placement of shunts on jack J4 located in the lower right hand corner of the board. Shunts placed on J4 make up the first (most significant) HEX digit of the board's starting address. A shunt corresponds to a "one", and no shunt corresponds to a "zero". This provides for HEX starting addresses 0000, 1000, 2000, ... F000.

I/O SELECTION

Jack J2, located in the lower right hand corner of the board, is used to select the I/O address to be used for Memory Mapping. The jack is labeled for the MS (most significant) and LS (least significant) halves of the I/O address. The 8 positions of J2 correspond to the 8 bits of the I/O address. A shunt corresponds to a "one"; no shunt corresponds to a "zero". Thus up to 256 unique addresses are possible.

I/O ADDRESS ENABLE (MAP)

The left most position of jack J3, labeled "MAP" and located in the lower right hand corner of the board, is used to Enable or Disable the I/O address. If Memory Mapping is to be used, the feature must be enabled by placing a shunt on the "MAP" pin of J3. With a shunt on the "MAP" pin of J3, the 370 board will respond to the I/O address selected by the J2 shunt placements causing the memory board's addresses to be mapped to the range corresponding to the starting address by the shunt placements on J4.

MEMORY MAP CONTROL (AND INITIALIZING ON)

The Memory Map register is an eight bit on board register that controls the "ON/OFF" state of the eight 4K blocks of the memory board. Bit 0 controls the "0" block, bit 1 the next block and so on. Thus for a board with a starting address selected on jack J4 of 0000, the map register bits control the address blocks as follows:

BIT	MEMORY ADDRESSES
0	0000-0FFF
1	1000-1FFF
2	2000-2FFF
3	3000-3FFF
4	4000-4FFF
5	5000-5FFF
6	6000-6FFF
7	7000-7FFF

INITIALIZATION

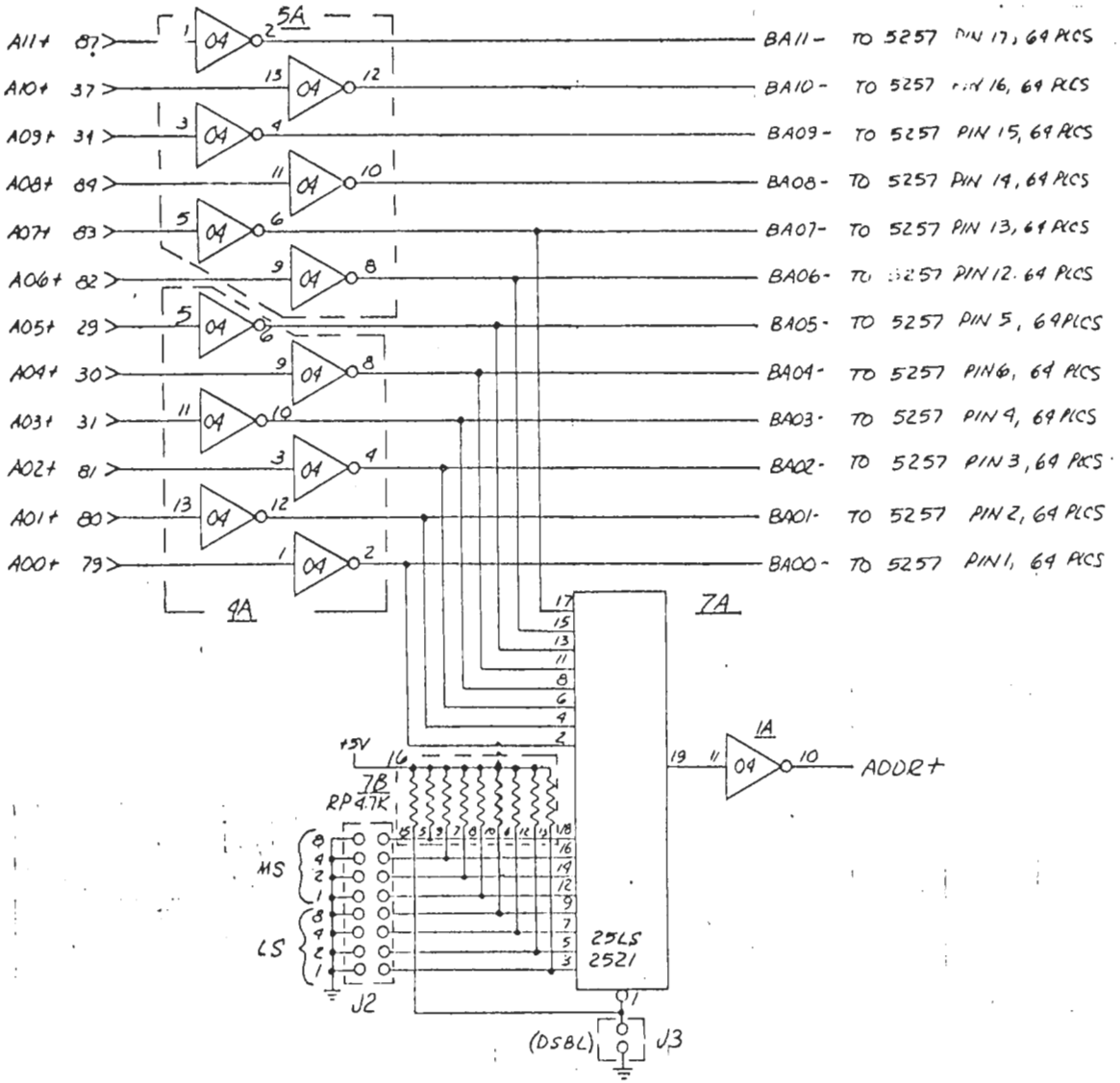
The "RESET" or "POWER ON CLEAR" signals clear the contents of the memory map register. The exception to this occurs if a shunt is placed on the "ON" position of jack J1; in this case upon the occurrence of "RESET" or "POWER ON CLEAR", the effect is as though all 1's (hexadecimal 'FF') were output to the memory map register initializing the entire board to the "ON" state. The "ON" feature simply provides a means of forcing a board fully "ON" at the system start-up. If memory mapping is used and more than one board in the system is set for the same address range, at most only one of the boards should have a shunt on the "ON" position of jack J1. After system start-up, the "ON" feature is overridden by the first map command received by the board and the contents of the memory map register controls the "ON/OFF" states of the 4K blocks on the memory board.

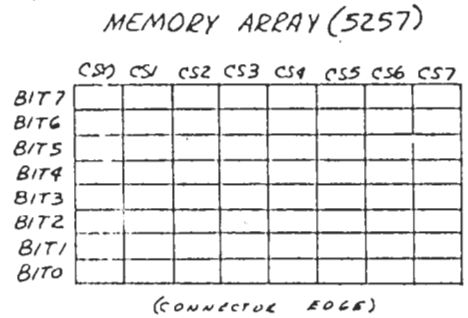
PWR/MWR

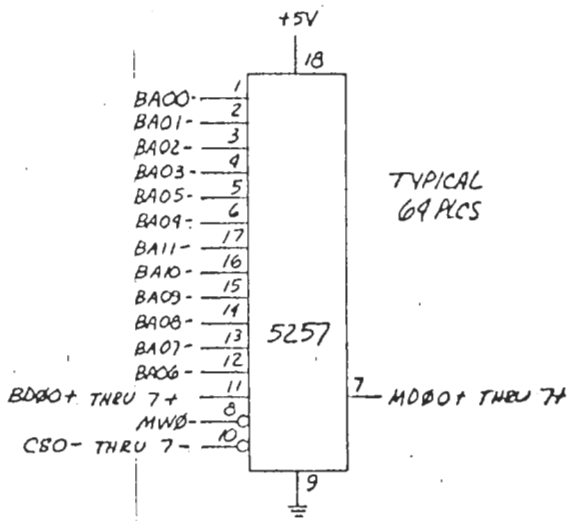
This selection is made on jack J1, located in the lower left hand portion of the board. One shunt should be placed on either PWR to select Processor Write or MWR to select Memory Write. Systems with front consoles (e.g., IMSAI) should use MWR. Caution - Install only one shunt - never both PWR and MWR.

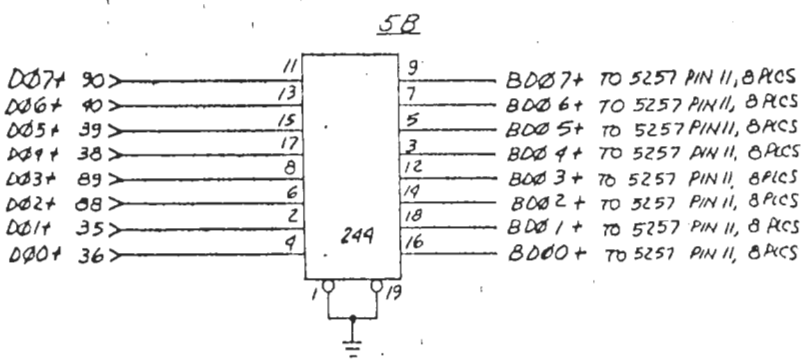
PHANTOM

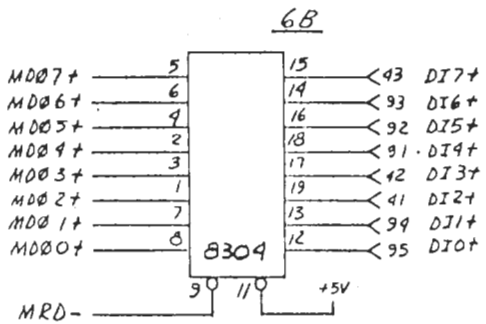
The Phantom Line (for systems using ROM with this feature) is enabled by placing a shunt on the PH pins on jack J1. If this feature is not used, it is recommended that this shunt not be installed.





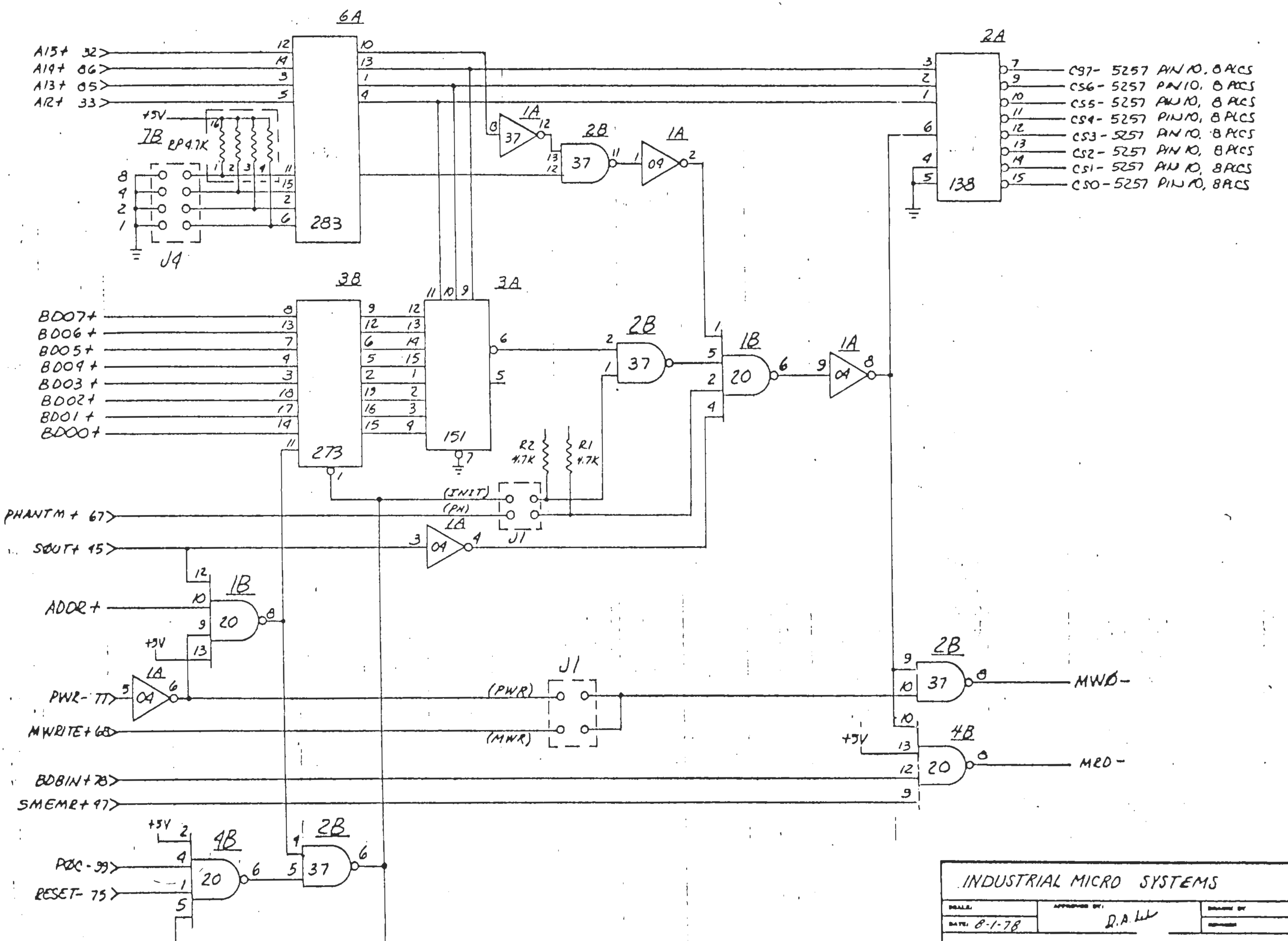






NOTE: ALL IC'S ARE 74LS EXCEPT 6B & MEMORY.

INDUSTRIAL MICRO SYSTEMS		
SCALE: ~	APPROVED BY: D.A. LANE	DRAWN BY
DATE: 8-1-78		SIGNED
32K STATIC RAM MEMORY		
L00370		SHEET NUMBER 1 OF 2



INDUSTRIAL MICRO SYSTEMS

DATE: 8-1-78

D.A.

32K STATIC RAM M ORY